Overcoming the Mixed Signal Chip Simulation Limits of the EF Anti-Jitter Circuit

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***Abstract*—The EF-AJC is a mixed signal circuit operating with GHz sawtooth waveforms and feedback time constants of a few milliseconds. Jitter has to be modeled to sub-picosecond accuracy. Conventional time-step simulation is impossible in reasonable time. The paper addresses the validity of the 'indirect' simulation methods that have to be used. The 'simulations' are compared with 500MHz results from a Fujitsu Micro-Electronics test chip. This 90nm chip suppresses jitter by 8 times. The estimated residual jitter is less than an estimated 2 to 5ps.**

I. INTRODUCTION

The Anti-Jitter Circuit (AJC) is a simple 'mixed signal' circuit that can be embedded on a chip to reduce time jitter and phase noise. It was first announced at the EFTF in 1996 and has been significantly advanced since then [1] to [13]. AJC technology is being continuously developed by Toric Limited for a wide range of potential applications in most areas of consumer and professional electronics.

'Mixed Signal' means that the circuit is partly analogue and partly digital. In this respect the AJC is similar to the PLL (Phase-Locked Loop), but it does not have a VCO (Voltage Controlled Oscillator).

Chip manufacturers require chip designs are 100% simulated before the design is released for manufacture. Chip re-runs are very costly and time consuming. The aim of simulation is to avoid re-runs and achieve 'right first time' manufacture. Potentially the AJC is better than the PLL in this respect because there is no on-chip VCO. On-chip PLLs often require re-runs because of the difficulty in getting the on-chip VCO frequency range correct on the first IC run.

The original basic AJC (Auto NRC) is relatively easy to simulate for applications where the analogue RC time constants are not long. Typically a transistor level simulation in SPICE will take about half an hour to determine AJC suppression down to one tenth of carrier input frequency.

The EF-AJC (Enhanced Feedback-AJC) technique [8] was announced in 2004 [10]. This technique improves both suppression and lowest frequency of suppression. A 1GHz 'EF-AJC' in high level 'behavioural' simulation has been shown to give good (>20dB) suppression down to a suppression bandwidth limit of a few kHz. A SPICE time-step simulation requires picosecond steps for up to a millisecond. This is more than a billion (10^9) program steps for each of the thirty or so nodes of the EF-AJC. Without special measures, a simulation to the normally required standard would take several months.

Furthermore we have found that SPICE simulation does not always model all the analogue circuits well enough to give correct representation of some practical AJC circuit implementations. For example the 'grounded-base charge pump' is sometimes incorrectly modeled. (The 'charge packets' out of the collector can appear to differ substantially in size from those going into the emitter.) A further problem occurs if the SPICE adaptive step size operation is enabled. Then an FFT does not always discern the additional suppression deriving from the EF technique.

II. EF-AJC PRINCIPLES

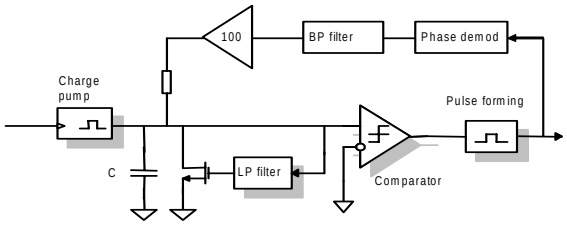

Figure 1. Principle of the EF Anti-Jitter Circuit

The EF-AJC in Fig.1 has an Extra Feedback (EF) loop around a Basic AJC. It lowers the cut-off frequency, and improves the jitter suppression, intrinsic noise and residual jitter.

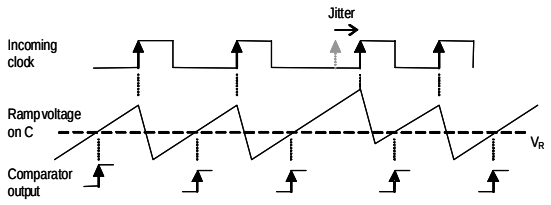

Figure 2. Principle of AJC jitter suppression.

The Basic AJC has a floating charge integrator that creates a ramp waveform, with local feedback to maintain

the operating point. Fig.2 shows this. The comparator output has much reduced jitter (on the rising edge).

A Basic AJC typically has about twenty components or circuit nodes. An EF-AJC has typically less than forty components or circuit nodes.

III. Jitter Estimates from the Phase Noise Spectrum

For any source the spectrum of its time jitter is the same as the spectrum of its phase noise. A typical phase noise spectrum can be bounded by the template shown in Fig. 3.

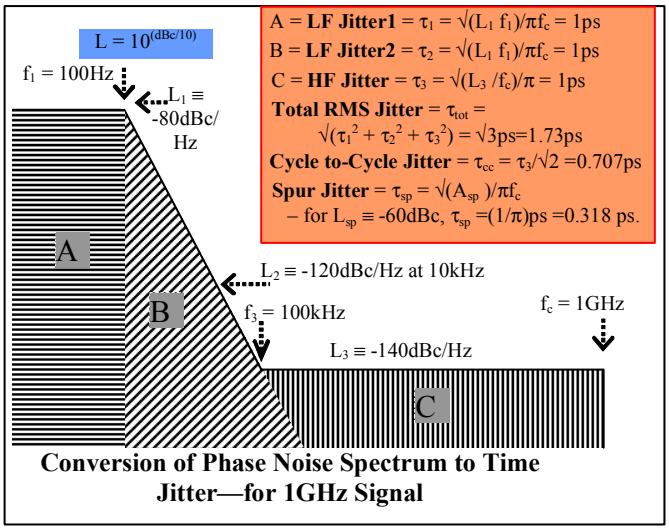

Figure 3. Idealised noise template suitable for calculation of residual EF-AJC jitter.

The total time jitter is the square root of the area under the phase noise envelope times an appropriate scale factor. The scale factor is the reciprocal of the product of π and the carrier frequency. The template shown covers three contributions A, B and C. Each of these has a finite value and so the total time jitter has a finite value in this case.

Note that the time jitter values τ of the contributions A, B and C have to be combined according to the 'Root-Sum-of-the-Squares' (RSS) process. The RSS process causes the strongest noise to dominate and suppress the smaller contributions, which then need not be calculated accurately.

It is interesting to note that contributions A and B are equal for the case shown. In most cases this is a good assumption.

The combination of A and B is the total LF jitter. The new EF–AJC technique typically gives substantial (greater than 20dB) reduction in the LF jitter.

The Basic AJC focuses on the reduction of the HF jitter, area C in Fig. 3. Often this is the dominant source of total jitter. If this is the case the EF technique is not needed. An adequate jitter reduction may be obtained with the basic AJC alone.

When the parameter of interest the 'cycle-to cycle' jitter (sometimes confusingly called 'peak-to-peak' jitter) is the contribution of area C nearly always dominates. This is because the cycle-to-cycle measurement process imposes a sine of frequency amplitude filter on the noise spectrum. There is a zero at zero-frequency which in most if not all cases removes the LF noise contributions A and B. The effect of the filter is to reduce its mean level of C by 3dB. The measured cycle-to-cycle jitter τ_{cc} is therefore the HF jitter τ_3 reduced by $\sqrt{2}$ as shown in Fig.3.

The template in Fig. 3 has been chosen so that the noise contributions A, B, and C are all equal to 1ps. By a coincidence it is a good target template for n EF AJC operating at 1GHz. The scaling factors for a change in operating factor are shown in the figure.

IV. Time-Step Modeling with SPICE

Fig. 4 shows a SPICE simulation model of the EF-AJC set up for the purpose of time-step simulation of the transient response. SIMetrix SPICE was used.

The circuit uses a mixture of real and idealised components. This is a balance between accuracy of representation and speed of operation of the circuit. The main blocks of the EF-AJC of Fig 1 can be identified in the detailed circuit implementation in Fig. 4.

The two monostables shown are both entirely made up of standard digital gates. In practice the monostable delay time is set by choosing the appropriate number of gates in one of the parallel paths.

Current source Q_1 models the charge pump and current source Q_2 models the controlled discharge path that generates the long slope of the integrator capacitor sawtooth waveform.

The DC stabilization loop has shorter time constants than would normally be used in practice. The main change is that R_4 has been made 27k rather than the recommended 270k. This improves the AJC startup time for simulation but at the cost of raising the lowest suppression frequency by about ten times. The circuit shown in Fig. 4 has a simulation time of just over a minute seconds for a time record of about twenty microseconds.

The EF feedback loop is AC coupled through capacitor C_6. This sets the lowest suppression frequency when the loop is closed. Note that an increase of this capacitor by ten times allows the EF loop gain to be increased by nearly ten times before instability sets in. The consequence is that the lowest suppression frequency can then be lowered by nearly one hundred times.

C_2 is the AJC integrator capacitor. The Basic AJC (with the EF loop gain set to zero) has a lowest suppression frequency determined mainly by C_2 and R_2. The inner loop gain raises the cut-off frequency of the core AJC. But at the same time it reduces the noise contributions from the core AJC. When the EF loop is applied the higher core AJC does not matter and its noise and jitter contributions are further reduced.

The key part of the EF feedback circuit is the circuit part containing the three diodes D1, D2 and D3. It is a

'mean-of-peaks' circuit. It is fed by out of phase balanced signals from E4 and E8. This EF bridge phase demodulator circuit has the important function of suppressing the input signal carrier frequency component at this point by about 40dB or more. It allows an EF feedback loop gain of at least 40dB to be achieved.

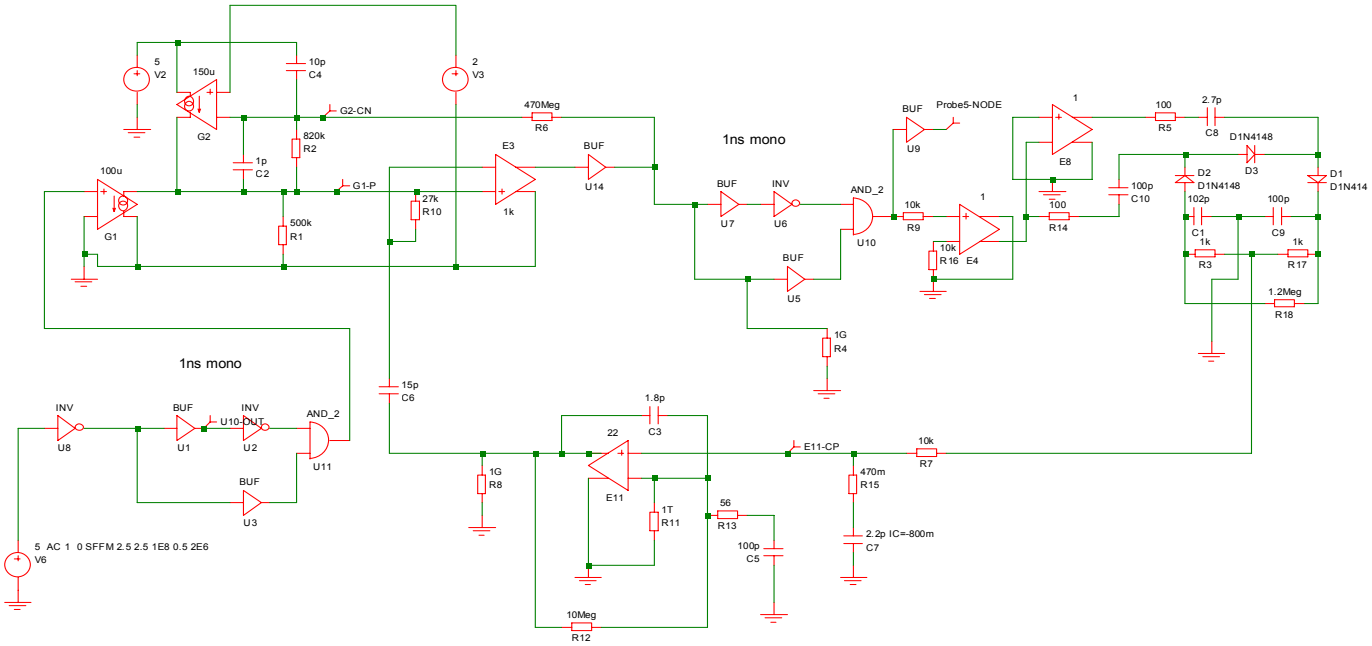

Figure 4. EF-AJC circuit for the purpose of: time step modelling.

Fig. 5 shows the start-up time response of the AJC in Fig. 4 with 'optimum' EF loop gain set by amplifier E11 having a gain of 22. G1-P is the integrator capacitor C2 waveform. Note that the AJC output 'Probe5 Node' is present just after 4µs. U10-OUT' is the input signal acting as a time reference. G2-CN (blue) is the voltage control to the discharge current source G2. E11-CP is the output voltage of the EF feedback loop. Note that this achieves its final value after about 5µs.

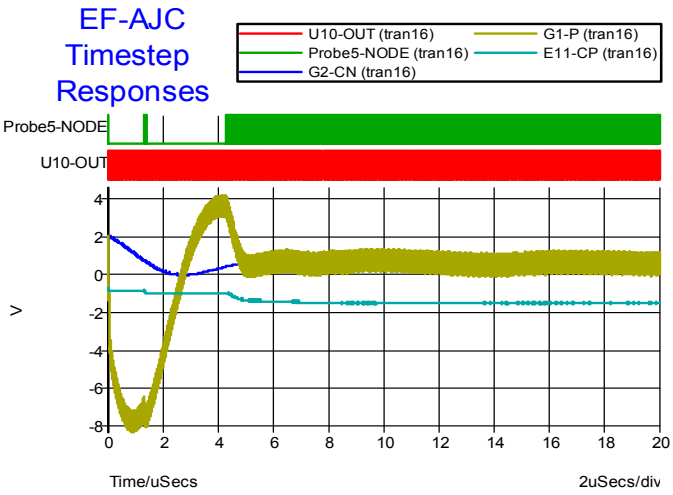

Figure 5. EF-AJC initial start-up time responses.

Fig. 6 expands the EF-AJC time responses at about 19.5µs. The 10MHz modulation with index of 0.5 can be seen on the integrator capacitor waveform G1-P.

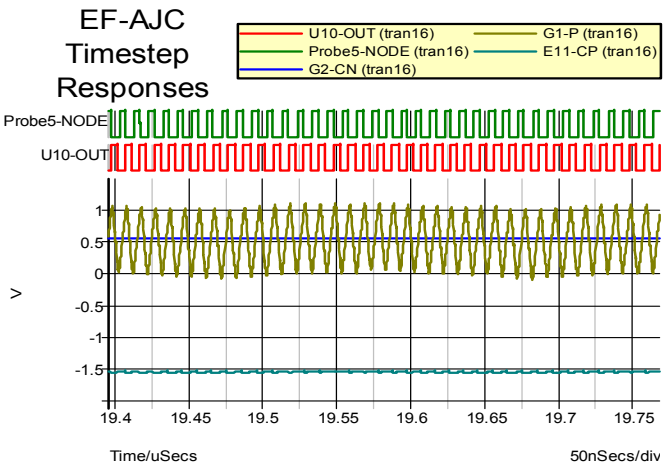

Figure 6. EF-AJC initial start-up time responses expanded at 19.5µs.

Note that the EF loop shortens the acquisition or start-up settling time. This effect was a surprise. It was assumed that the long time constant generated by the EF feedback would dominate this process. It obviously does not slow up acquisition.

Fig. 7 and Fig. 8 show the time responses when the EF loop gain is zero. They can be compared directly to Fig. 5 and Fig. 6 respectively. Note that the settling time to continuous

AJC output is at least doubled to 8µs. This is also a short disappearance of the output just after 12µs.

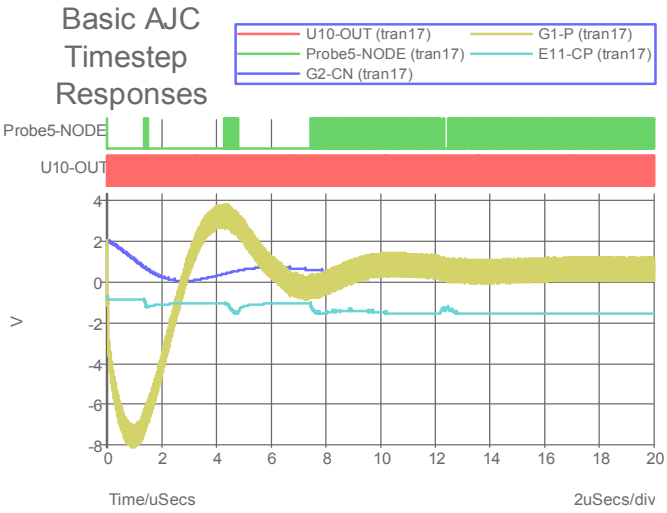

Figure 7. Start-up time responses with EF feedback gain of zero.

Note that the charge pump control voltage also takes longer to settle. Thus the EF loop does speed up settling after a frequency step.

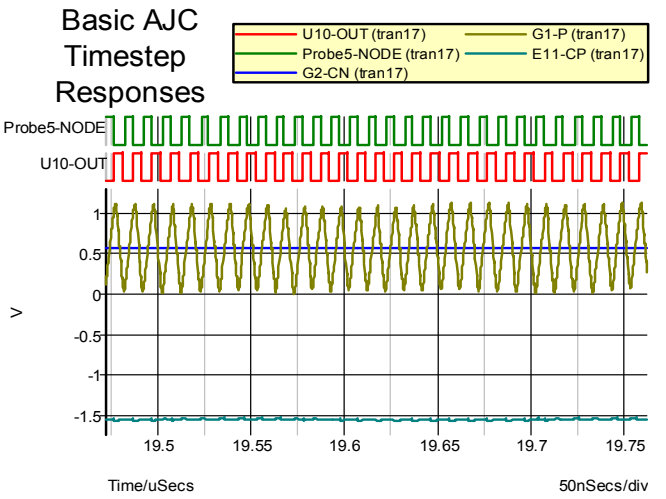

Figure 8. Start-up time responses with EF feedback gain of zero.after about 19.5µs.

V. High-Level System Modeling in SPICE

Fig. 9 shows the circuit diagram used for high level SPICE simulation of the EF-AJC. It has the same circuit topology as Fig. 4 but the diode EF circuit has been replaced by an equivalent circuit suitable for high level modelling rather than for time-step modelling.

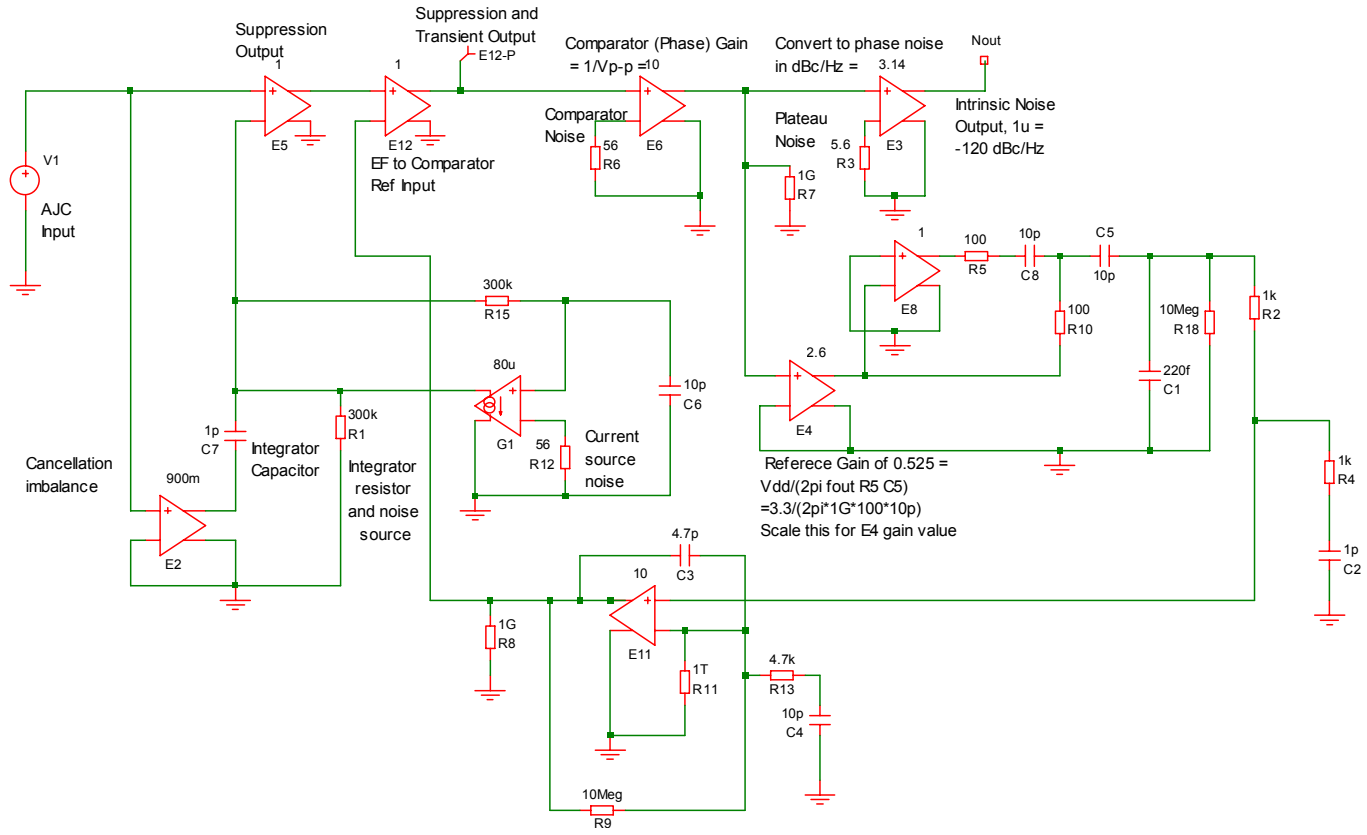

Figure 9. EF-AJC circuit for the purpose of: high-level modelling.

The suppression transfer function and the internal 'intrinsic' noise are shown in Fig 10 and Fig. 11 respectively. In each of these figures the performance with and without EF feedback is compared.

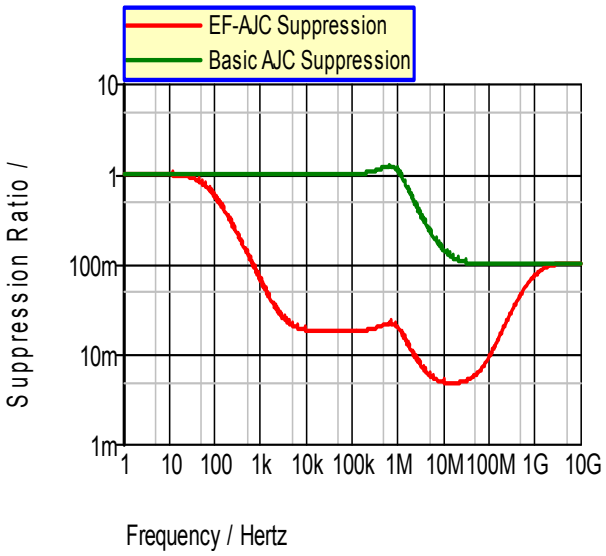

Figure 10. EF-AJC suppression with and withot EF supression. 100m is 20dB suppression. 10m is 40dB suppession)

Fig. 10 shows that the addition of the EF feedback gives a dramatic improvement of the overall AJC suppression. The lowest suppression frequency is reduced from 1MHz to 100Hz. The suppression is increased from an initial assumed 20dB to over 40dB at some frequencies.

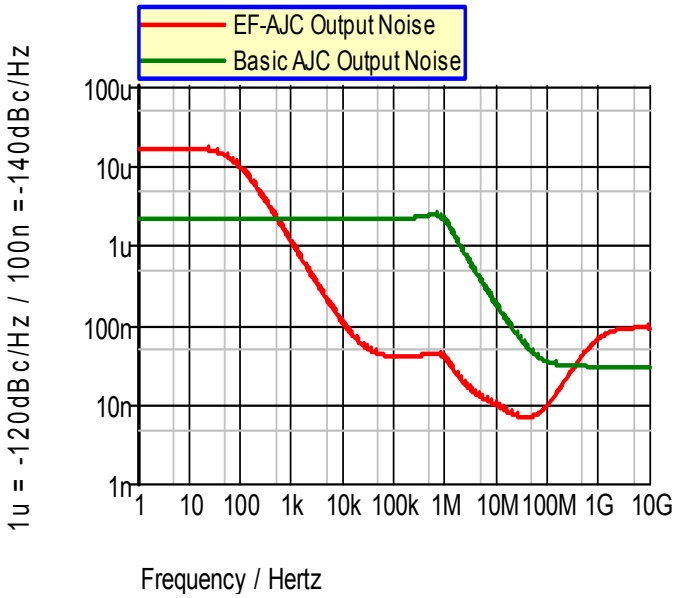

Figure 11. EF-AJC suppression with and withot EF supression. 1u is -120dBc/Hz.. 100n is -140dBc/Hz. ..

The simulations assumed an input carrier frequency of between 200MHz and 1GHz. The plots are not valid above the carrier frequency whatever it is. In practice one has aliased sidebands appearing around the harmonics of the carrier frequency.

Fig. 11 shows that when the EF loop is switched on the intrinsic noise is considerably reduced at frequencies above about 500Hz. The phase noise limit is -120dBc/Hz at 1 kHz. This is better than typical LC VCO PLLs by about 20dB. In general the performance of on-chip PLLs is a further 10dB worse. The EF-AJC appears to be able to out-perform any on-chip PLL in terms of low phase noise.

VI. Simulation Results

Fig. 12 shows Cadence SpectreRF simulation results for the EF AJC shown in Fig. 4. SpectreRF first simulates the circuit in time-step mode and detects when the circuit has sufficiently settled for a second high level simulation step. The second step extracts the linearised small signal transfer functions of every component required for high level simulation. Essentially it automatically creates the equivalent circuit shown in Fig. 9. This equivalent circuit with 'back extracted' values is what is finally simulated.

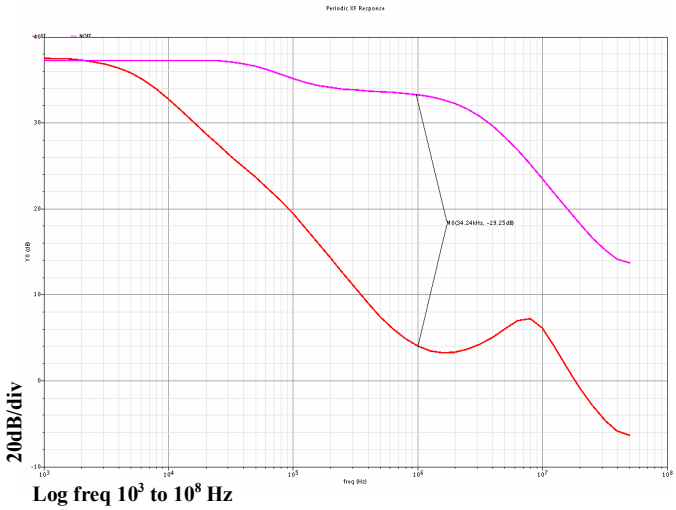

Figure 12. EF improvement = 29dB at 10^6 Hz simulated by Cadence SpectreRF

From Fig. 12 we can see that the EF loop give a thirty dB benefit in additional suppression at 1MHz.

The general shape of the suppression curves is similar to those predicted with the simple SIMetrix SPICE simulator as shown in Fig. 10.

Thus the simple simulation method is to a considerable extent validated by SpectreRF. It can be used for initial design optimization. Final validation is achieved with higher confidence by the use of SpectreRF.

VII. AJC Jitter Suppression Results Fom A Silicon Test Chip

Fig. 13 shows on an oscilloscope the time jitter suppression of a dual basic AJC test chip manufactured by Fujitsu in 90nm CMOS technology. The operating frequency was 500MHz. The top wave form is the original

input signal. The middle waveform is the output from the comparator of the first AJC. The bottom waveform is the output from the comparator of the second AJC in series with the first AJC. A time jitter suppression of about eight times can be seen.

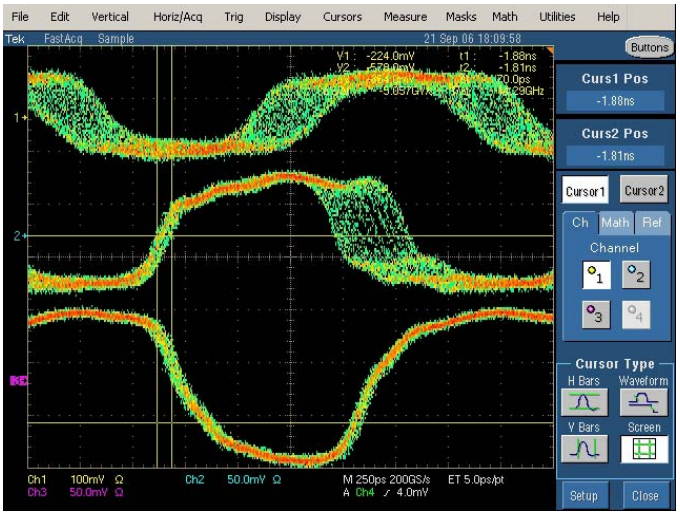

Figure 13. Fujitsu 90nm AJC test chip reduces jitter by 8 times at 500MHz.

The residual jitter could not be measured with the equipment available. Fig. 13 shows a measured RMS jitter of 25ps. Investigation showed that most of the apparent jitter is being picked up on the oscilloscope probes.

The residual jitter can be estimated by the method summarized in Fig. 3. However the phase noise measuring equipment used had a noise floor of -127dBc/Hz. This corresponds to a time jitter of about 10 to 15ps. The simulated phase noise plot indicates a jitter of less than 2ps. The safe estimate is 2 to5ps.

VIII. Virtual Demonstrator Chip

A 'Virtual Demonstrator' chip design (with Saul Research) is being used in the more detailed EF-AJC design investigations. It is a full circuit simulation using the austriamicrosystems 180nm CMOS process design rules and library devices. It stops short of inclusion of layout parasitics derived by 'back extraction'. The demonstrator also provides a 'reference model' for the AJC simulation to the level required for chip manufacture. .

IX. Conclusion

The results and analysis above indicate that the EF-AJC has the potential to replace practically all on-chip PLLs with significant improvements in cost and performance. Design cost is intrinsically less. There are no design iterations required to get the VCO 'on-tune' in spite of process variations. There are no inductors needed in the VCO. The phase noise of a poor ring oscillator VCO can be improved to be better than an LC VCO.

Without the EF loop a high power comparator has to be used in the AJC if the overall jitter is to be kept low. The EF-feedback loop suppresses noise in the AJC comparator. A lower power comparator can then be used. .

In the limit a comparator can be the first part of a standard logic gate. This can be very low power. Thus the current in the basic AJC integrator then is the power determining factor. In the 100MHz examples above the integrator current is about 0.1 ma. This scales to about 1ma at 1GHz.

The AJC is proving to be one of the most significant circuit developments since the PLL. The EF-AJC can exceed PLL performance for jitter, phase noise noise and power in most applications.

Acknowledgment

We would like to thank Andrew Beckett and Ian Clifford of Cadence at Bracknell for the SpectreRF simulation results shown in Fig. 12.

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